

WHAT IS CLAIMED IS:

1 1. A method for forming bit line and storage node contacts for a dynamic
2 random access device, the method comprising:
3 providing a substrate, the substrate having a bit line region and a capacitor
4 contact region;
5 forming at least a first gate structure and a second gate structure overlying the
6 substrate, the first gate structure including an overlying first cap, the second gate structure
7 including an overlying second cap, the first gate structure being spaced by the bit line region
8 to the second gate structure, the capacitor contact region being coupled to the first gate
9 structure;
10 forming a conformal dielectric layer overlying the first gate structure, the
11 second gate structure, the bit line region, and the capacitor contact region;
12 forming an interlayer dielectric material overlying the conformal dielectric
13 layer;
14 planarizing the interlayer dielectric material;
15 forming a masking layer overlying the planarized interlayer dielectric
16 material;
17 exposing a continuous common region within a portion of the planarized
18 interlayer dielectric material overlying a portion of the first gate structure, a portion of the
19 second gate structure, a portion of the bit line region, and a portion of the capacitor contact
20 region;
21 performing a first etching process to remove the exposed portion of the
22 planarized interlayer dielectric layer;
23 performing a second etching process to remove a portion of the conformal
24 dielectric layer on the bit line region and to remove a portion of the conformal dielectric layer
25 on the capacitor contact region while using other portions of the conformal layer as a mask to
26 prevent a portion of the first gate structure and a portion of the second gate structure from
27 being exposed; depositing a polysilicon fill material within the continuous common region
28 and overlying the bit line region, the capacitor contact region, the first gate structure, and the
29 second gate structure to cover portions of the bit line region, the capacitor contact region, the
30 first gate structure, and the second gate structure to a predetermined thickness;
31 planarizing the polysilicon fill material to reduce the predetermined thickness
32 and to simultaneously reduce a thickness of a portion of the interlayer dielectric material;

33 continuing the planarization of the polysilicon fill material and the interlayer
34 dielectric material; and
35 exposing a portion of the first gate structure and a portion of the second gate
36 structure while leaving portions of the polysilicon fill material on the portion of the capacitor
37 contact region and the portion of the bit line region, whereupon the polysilicon fill material
38 on the portion of the capacitor contact region is isolated from the polysilicon fill material on
39 the portion of the bit line region.

1 2. The method of claim 1 wherein the first gate structure including an
2 overlying first tungsten silicide layer and the second gate structure including an overlying
3 second tungsten silicide layer.

1 3. The method of claim 1 wherein the conformal dielectric layer is silicon
2 nitride.

1 4. The method of claim 1 wherein the planarizing includes a chemical
2 mechanical polishing process and/or an etch back process.

1 5. The method of claim 1 wherein the wherein the polysilicon fill
2 material is an in-situ doped polysilicon material or an amorphous silicon material or an in-
3 situ-doped amorphous silicon material or a polysilicon material or a doped polysilicon
4 material.

1 6. The method of claim 1 wherein the wherein the polysilicon fill
2 material in the portion capacitor contact region is electrically isolated from the first gate
3 structure and the second gate structure and the polysilicon fill material in the portion of the
4 bit line region is electrically isolated from the first gate structure and the second gate
5 structure.

1 7. The method of claim 1 wherein the continuous common region is
2 shaped as an "I" configuration.

1 8. The method of claim 1 wherein the continuous common region is
2 shaped as a "T" configuration.

1 9. The method of claim 1 wherein the first gate structure and the second
2 gate structure are spaced by the bit line region, the space being about 0.135 microns and less.

1 10. The method of claim 1 wherein the first gate structure is characterized
2 by a design dimension of 0.13 micron and less the second gate structure is characterized by a
3 design dimension of 0.13 micron and less.

1 11. A method for forming a self aligned contact region for a dynamic
2 random access memory device, the method comprising:
3 providing a semiconductor substrate, the semiconductor substrate having a cell
4 region and a peripheral region;

5 forming at least a first gate structure, a second gate structure, a third gate
6 structure, and a fourth gate structure in the cell region and forming a gate structure in the
7 peripheral region, the first gate structure including an overlying first cap, the second gate
8 structure including an overlying second cap, the third gate structure including an overlying
9 third cap structure, the fourth gate structure including an overlying fourth cap structure, the
10 second gate structure being spaced by a bit line region to the third gate structure, the first gate
11 structure being spaced by a first capacitor contact region to the second gate structure, the
12 third gate structure being spaced by a second capacitor contact region to the fourth gate
13 structure;

14 forming a conformal dielectric layer overlying the first gate structure, the
15 second gate structure, the third gate structure, the fourth gate structure, the bit line region, the
16 first capacitor contact region, and the second capacitor contact region in the cell region and
17 the gate structure in the peripheral region;

18 forming an interlayer dielectric material overlying the conformal dielectric
19 layer;

20 planarizing the interlayer dielectric material;

21 forming a masking layer overlying the planarized interlayer dielectric
22 material;

23 exposing a continuous common region within a portion of the planarized
24 interlayer dielectric material overlying the first gate structure, the second gate structure, the
25 third gate structure, the fourth gate structure, the bit line region, the first capacitor contact
26 region, and the second capacitor contact region while maintaining the planarized interlayer
27 dielectric material overlying the gate structure in the peripheral region;

28 performing an etching process to remove the exposed portion of the planarized
29 interlayer dielectric layer in the continuous common region to expose the bit line contact, the

30 first capacitor contact region, and the second capacitor contact region while using portions of
31 the conformal layer as a mask to prevent any conductive portions of the first gate structure,
32 the second gate structure, the third gate structure, and the fourth gate structure from being
33 exposed;

34 depositing a polysilicon fill material within the continuous common region
35 and overlying the bit line region, the first capacitor contact region, and the second capacitor
36 region, the first gate structure, the second gate structure, the third gate structure, and the
37 fourth gate structure to a predetermined thickness;

38 planarizing the polysilicon fill material to reduce the predetermined thickness
39 and to simultaneously reduce a thickness of a portion of the interlayer dielectric material to a
40 vicinity of an upper region of the first gate structure, the second gate structure, the third gate
41 structure, the fourth gate structure, and the gate structure;

42 continuing the planarization of the polysilicon fill material and the interlayer
43 dielectric material; and

44 exposing a portion of the first gate structure, a portion of the second gate
45 structure, a portion of the third gate structure, a portion of the fourth gate structure, and a
46 portion of the gate structure while leaving portions of the polysilicon fill material on the bit
47 line region, the first capacitor contact region and the second capacitor contact region,
48 whereupon the polysilicon fill material on the first capacitor contact region is isolated from
49 the polysilicon fill material on the bit line region and the polysilicon fill material on the
50 second capacitor contact region is isolated from the polysilicon fill material on the bit line
51 region.

1 12. The method of claim 11 wherein the first gate structure including an
2 overlying first tungsten silicide layer and the second gate structure including an overlying
3 second tungsten silicide layer, the third gate structure including an overlying third tungsten
4 layer, the fourth gate structure including an overlying fourth tungsten layer, and the gate
5 structure including an overlying tungsten layer.

1 13. The method of claim 11 wherein the conformal dielectric layer
2 comprises silicon nitride.

1 14. The method of claim 11 wherein the planarizing includes a chemical
2 mechanical polishing process and/or an etch back process.

1 15. The method of claim 11 wherein the wherein the polysilicon fill
2 material is an in-situ doped polysilicon material or an amorphous silicon material or an in-
3 situ-doped amorphous silicon material or a polysilicon material or a doped polysilicon
4 material.

1 16. The method of claim 11 wherein the wherein the polysilicon fill
2 material in the first capacitor contact region is electrically isolated from the first gate
3 structure and the second gate structure; wherein the polysilicon fill material in the bit line
4 region is electrically isolated from the second gate structure and the third gate structure; and
5 wherein the second capacitor contact region is electrically isolated from the third gate
6 structure and the fourth gate structure.

1 17. The method of claim 11 wherein the continuous common region is
2 shaped as an "I" configuration.

1 18. The method of claim 11 wherein the continuous common region is
2 shaped as a "T" configuration.

1 19. The method of claim 11 wherein the second gate structure and the third
2 gate structure are spaced by the bit line region, the space being about 0.135 microns and less;
3 and wherein the first gate structure, the second gate structure, the third gate structure, and the
4 fourth gate structure is characterized by a design dimension of 0.13 micron and less.